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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	9

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/730,039	Applicant(s) MOHAMED ET AL.	
	Examiner Aimee J Li	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 and 11-28 have been considered. Claims 1, 3, 9, 12-15, 17-21, and 23 have been amended as per Applicant's request. Claim 10 has been cancelled as per Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 7-9, 21-23, and 27-28 rejected under 35 U.S.C. 102(b) as being taught by Keckler et al., U.S. Patent Number 5,574,939 (herein referred to as Keckler).

4. Referring to claim 1, Keckler has taught a processor comprising:

   a. A first plurality of threads, each of said first plurality of threads comprising one of a second plurality of processing units (Keckler column 2, lines 3-17 and 22-38; Figure 1; Figure 2; and Figure 3);

   b. A fourth plurality of instruction packets, wherein each of said fourth plurality of instruction comprises a third plurality of issue groups (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; Figure 2; and Figure 3);

   c. Each of said first plurality of threads receiving a respective one of a third plurality of issue groups from a respective one of said fourth plurality of instruction packets (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; Figure 2; and Figure 3). In regards to Keckler, the "multiple

operations to be performed in parallel (Keckler column 1, lines 32-35)" is similar to the issue groups, which are "instructions...which can be executed in the same clock cycle (Applicant's Specification Page 2, lines 12-13)".

d. A respective one of said second plurality of processing units executing said third plurality of issue groups in a single clock cycle (Keckler column 3, lines 41-61 and Figure 1).

5. Referring to claims 2 and 22, Keckler has taught wherein each of said first, second, third, and fourth pluralities is equal to two (Keckler column 13, line 64 to column 14, line 2). In regards to Keckler, Keckler refers to multiple threads, instructions, issue groups, and execution units as cited above. Since "multiple" means more than one, it includes two.

6. Referring to claims 3 and 23, Keckler has taught wherein each of said fourth/first plurality of instruction packets comprises two issue groups (Keckler column 13, line 64 to column 14, line 2). In regards to Keckler, Keckler refers to multiple threads, instructions, issue groups, and execution units as cited above. Since "multiple" means more than one, it includes two.

7. Referring to claims 7 and 27, Keckler has taught wherein each one of said fourth/first plurality of instruction packets resides in a respective instruction cache and is addressed by a respective program counter (Keckler column 4, lines 28-43; column 5, lines 2-4 and 31-40; column 8, lines 26-44; column 8, line 66 to column 9, line 3; Figure 2; and Figure 3).

8. Referring to claim 8, Keckler has taught wherein each of said first, second, third, and fourth pluralities is equal to four (Keckler column 4, lines 28-43; column 5, lines 31-40; and Figure 2).

9. Referring to claim 9, Keckler has taught a method for improving performance of a VLIW processor comprising:

a. Dividing a first instruction packet into a first packet first issue group and a first packet second issue group (Keckler column 2, lines 3-19 and 22-38; Figure 1; Figure 2; and Figure 3);

b. Dividing a second instruction packet into a second packet first issue group and a second packet second issue group (Keckler column 2, lines 3-19 and 22-38; Figure 1; Figure 2; and Figure 3);

c. Providing said first packet first issue group to a first thread having a first thread processing unit and said second packet first issue group to a second thread having a second thread processing unit during a first clock cycle (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; column 3, lines 41-61; Figure 1; Figure 2; and Figure 3); and

d. Providing said first packet second issue group to said first thread having said first thread processing unit and said second packet second issue group to said second thread having said second thread processing unit during a second clock cycle (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; column 3, lines 41-61; Figure 1; Figure 2; and Figure 3).

10. Referring to claim 21, Keckler has taught a method for improving performance of a VLIW processor comprising:

a. Dividing each one of a first plurality of instruction packets into a second plurality of issue groups (Keckler column 2, lines 3-19 and 22-38; Figure 1; Figure 2; and Figure 3);

b. Providing each one of said second plurality of issue groups, in one of a third plurality of clock cycles, to a respective thread having a respective processing unit (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; column 3, lines 41-61; Figure 1; Figure 2; and Figure 3);

c. Executing said first plurality of instruction packets in said third plurality of clock cycles, wherein an issue group from each one of said first plurality of instruction packets is executed in one of said third plurality of clock cycles (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; column 3, lines 41-61; Figure 1; Figure 2; and Figure 3).

11. Referring to claim 28, Keckler has taught wherein said first plurality is equal to four (Keckler column 4, lines 28-43; column 5, lines 31-40; and Figure 2), and wherein each of said second and third pluralities is equal to two (Keckler column 13, line 64 to column 14, line 2). In regards to Keckler, Keckler refers to multiple threads, instructions, issue groups, and execution units as cited above. Since "multiple" means more than one, it includes two.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 4-6, 11-20, and 24-26 rejected under 35 U.S.C. 103(a) as being unpatentable over Keckler et al., U.S. Patent Number 5,574,939 (herein referred to as Keckler) in view of Applicant's admitted prior art (herein referred to as Prior Art).

14. Referring to claim 4, Keckler has not explicitly taught:

a. Wherein each of said plurality of instruction packets is 128/256 bits wide (Applicant's claims 4, 11, 16, and 24);

b. Wherein a first one of said two issue groups is 64/128 bits wide and a second one of said two issue groups is 48/112 bits wide (Applicant's claims 5, 12, 14, 17, 19, and 25); and

c. Wherein a first one of said two issue groups is 48/112 bits wide and a second one of said two issue groups is 64/128 bits wide (Applicant's claims 6, 13, 15, 18, 20, and 26).

15. However, Keckler has taught changes in form and details in the invention would not change the invention (Keckler column 13, line 64 to column 14, line 2). Prior Art has taught:

a. Wherein each of said plurality of instruction packets is 128/256 bits wide (Applicant's claims 4, 11, 16, and 24) (Prior Art page 3, lines 16-17 and page 4, lines 9-10).

b. Wherein a first one of said two issue groups is 64/128 bits wide and a second one of said two issue groups is 48/112 bits wide (Applicant's claims 5, 12, 14, 17, 19, and 25) (Prior Art page 4, line 20 to page 5, line 12).

c. Wherein a first one of said two issue groups is 48/112 bits wide and a second one of said two issue groups is 64/128 bits wide (Applicant's claims 6, 13, 15, 18, 20, and 26) (Prior Art page 4, line 20 to page 5, line 12).

16. In regards to Keckler and Prior Art, the size of the instruction packet and issue groups is not patentable material. See *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955) and *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976). A person of ordinary skill in the art at the time the invention was made would have recognized the larger bit widths are needed in VLIW instructions to ensure the multiple operations are contained in the VLIW instruction, thereby allowing multiple instructions to be executed in parallel. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the VLIW bit width of Prior Art in the device of Keckler.

Response to Arguments

17. Applicant's arguments filed 05 March 2004 have been fully considered but they are not persuasive.

18. Applicant argues in essence on pages 12-14

> "...Keckler does not teach, suggest, or disclose instruction packets comprising a plurality of issue groups wherein each issue group is sent separately to the processor for execution...
>
> ...
>
> ...Keckler does not teach, disclose, or suggest the limitation of preprocessing each instruction set by dividing an instruction set into a plurality of issue groups

and sending an issue group from each separate instruction set to a separate processing unit for processing during each clock cycle..."

19. This has not been found persuasive. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., see above highlighted arguments) are not explicitly recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Applicant's claims do not explicitly recite the limitations recited in the arguments and only hint or imply the limitations at best. The language used in the claims leaves broader interpretations available, as is shown below in an explanation of how the Keckler reference still reads upon the amended claims, specifically the independent claims.

20. Referring to claim 1, Keckler has taught a processor comprising:

a. A first plurality of threads, each of said first plurality of threads comprising one of a second plurality of processing units (Keckler column 2, lines 3-17 and 22-38; Figure 1; Figure 2; and Figure 3).

i. Keckler shows in Figure 1 a plurality of threads, namely Thread A, Thread B, and Thread C.

b. A fourth plurality of instruction packets, wherein each of said fourth plurality of instruction comprises a third plurality of issue groups (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; Figure 2; and Figure 3).

i. Keckler shows in Figure 1 multiple instruction packets which are the multiple rows in each thread. Each row in Keckler's Figure 1 has multiple

individual operations handled by a different unit, which are represented by the columns.

c. Each of said first plurality of threads receiving a respective one of a third plurality of issue groups from a respective one of said fourth plurality of instruction packets (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; Figure 2; and Figure 3). In regards to Keckler, the "multiple operations to be performed in parallel (Keckler column 1, lines 32-35)" is similar to the issue groups, which are "instructions...which can be executed in the same clock cycle (Applicant's Specification Page 2, lines 12-13)".

i. Keckler shows in Figure 1 each thread has received an issue group from a VLIW instruction. As stated above, each column in the grid shown in Keckler's Figure 1 is a processing unit, or separate issue group when in instruction format, and each row represents a select VLIW instruction.

d. A respective one of said second plurality of processing units executing said third plurality of issue groups in a single clock cycle (Keckler column 3, lines 41-61 and Figure 1).

i. Keckler shows in Figure 1 multiple processing units executing a select issue group. As stated above, each column in the grid shown in Keckler's Figure 1 is a processing unit, or separate issue group when in instruction format, and each row represents a select VLIW instruction.

21. Referring to claim 9, Keckler has taught a method for improving performance of a VLIW processor comprising:

a. Dividing a first instruction packet into a first packet first issue group and a first packet second issue group (Keckler column 2, lines 3-19 and 22-38; Figure 1; Figure 2; and Figure 3).

   i. Keckler has shown in Figure 1 that each VLIW instruction represented by a row can be divided into groups, represented by the columns. For example, Thread A has a first instruction packet in the second row which is divided into groups A3 and A4.

b. Dividing a second instruction packet into a second packet first issue group and a second packet second issue group (Keckler column 2, lines 3-19 and 22-38; Figure 1; Figure 2; and Figure 3).

   i. Keckler has shown in Figure 1 that each VLIW instruction represented by a row can be divided into groups, represented by the columns. For example, Thread B has a second instruction packet in the second row which is divided into groups B6 and B7.

c. Providing said first packet first issue group to a first thread having a first thread processing unit and said second packet first issue group to a second thread having a second thread processing unit during a first clock cycle (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; column 3, lines 41-61; Figure 1; Figure 2; and Figure 3).

   i. Keckler has shown in Figure 1 during clock cycle 3, which is a first clock cycle, groups A3 and B6 are executed.

d. Providing said first packet second issue group to said first thread having said first thread processing unit and said second packet second issue group to said second thread having said second thread processing unit during a second clock cycle (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; column 3, lines 41-61; Figure 1; Figure 2; and Figure 3).

i. Keckler has shown in Figure 1 during clock cycle 4, which is a second clock cycle, groups A4 and B7 are executed.

22. Referring to claim 21, Keckler has taught a method for improving performance of a VLIW processor comprising:

a. Dividing each one of a first plurality of instruction packets into a second plurality of issue groups (Keckler column 2, lines 3-19 and 22-38; Figure 1; Figure 2; and Figure 3).

i. Keckler shows in Figure 1 represents each instruction packet as a row and each column divides the rows into a plurality of issue groups. For example, there are three instruction packets in Thread A, since there are three rows, and Thread A has issue groups A1 and A2 in row 1; issue groups A3, A4, A5, and A6 in row 2; and issue groups A7 and A8 in row 3.

b. Providing each one of said second plurality of issue groups, in one of a third plurality of clock cycles, to a respective thread having a respective processing unit (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; column 3, lines 41-61; Figure 1; Figure 2; and Figure 3).

i. Keckler shows in Figure 1 that in the separate cycles that the provided issue groups are executed in an interleaved manner, meaning that as many issue groups as possible are executed by the processing units.

c. Executing said first plurality of instruction packets in said third plurality of clock cycles, wherein an issue group from each one of said first plurality of instruction packets is executed in one of said third plurality of clock cycles (Keckler column 1, lines 32-39, 45-49, and 53-67; column 2, lines 3-19 and 22-38; column 3, lines 41-61; Figure 1; Figure 2; and Figure 3).

i. Keckler shows in Figure 1 the multiple issue groups are executed, since each issue group represents a separate processing unit.

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

24. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
May 13, 2004

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